

at least one conductive member disposed along at least a portion of the row, said conductive member being associated with the row and making contact with the sources of the memory cells of the portion of the row, said conductive member being self-aligned with the memory cells of said portion of the row.

2. The non-volatile memory array of claim 1, wherein:

said plurality of memory cells includes a first row of memory cells and a second row of memory cells adjacent to the first row, each of the memory cells along a portion of the first row sharing a common source with at least one memory cell of the second row; and

said conductive member is disposed along at least a portion of the first and second rows, said conductive member being associated with the first and second rows and making [and makes] contact with the common sources of the memory cells in said portion of the rows, the contact of said conductive member being self-aligned with the memory cells of said portion of the rows.

*Sub B3*  
A 1  
Cont.  
*A 2*  
13. (Amended) In a flash erasable EPROM, a compact array, comprising:

[a substrate;]

a first flash erasable electrically programmable read-only memory (EPROM) cell formed on [the] a substrate, and including a first cell top, a first cell first side, and a second cell second side opposite to the first cell first side;

a first cap insulator formed over the first cell top of said first flash EPROM cell;

a first insulating sidewall formed on the first side of the first flash EPROM cell;

and

a conductive member disposed on at least a portion of said first insulating sidewall and making contact with a contact portion of the substrate adjacent to the first insulating sidewall, wherein said conductive member is associated with first row of memory cells to which the first flash EPROM belongs and that said conductive member enables the selective erasing of the memory cells of the first row during an erase operation.

*Sub B4*

17. (Amended) The compact array of claim 13, including:  
a second flash EPROM cell formed adjacent to the first flash EPROM cell, the second flash EPROM cell including a second cell top, a second cell first side and second cell second side, the second cell second side opposing the first cell first side across the contact portion of the substrate;

*G3*  
a second cap insulator formed over the second cell top of said second flash EPROM cell;

a second insulating sidewall formed on the second side of the second flash EPROM cell; and

said conductive member is disposed on at least a portion of said second insulating sidewall, wherein said conductive member is also associated with a second row of memory cells adjacent to the first row, and that said conductive member enables the selective erasing of the memory cells of the first row, second row, or both first and second rows during an erase operation.

*Sub B5*  
*G4*  
20. (Amended) In a flash EPROM memory device formed on a semiconductor substrate, an array configuration, comprising:

a plurality of flash EPROM cells arranged in an array having a plurality of rows extending in a row direction; and

a plurality of source [contacts formed along at least one row of the array, each said source contact being separated from an adjacent source contact by a substrate isolation region; and

a source] connecting [member] members extending in the row direction, each of said source connecting members disposed over, and making contact with, [said plurality of source contacts] sources of memory cells of each adjacent pair of row,

wherein each of said source connecting members enabling the selective erasing of the memory cells of one or both of the corresponding rows during an erase operation.

21. (Amended) The array configuration of claim 20, wherein:

[said plurality of source contacts are formed along row pairs, each said source contact being shared by one flash EPROM cell of one row of the row pair and one flash EPROM cell of the other row of the row pair] said source connecting members enable the selective erasing of the memory cells of one or more of the row pairs during an erase operation.

22. (Amended) The array configuration of claim 20, including:

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a plurality of bit line contacts formed along at least one row of the array, opposite to said source [contacts] connecting members.

23. (Amended) *B* The array configuration of claim 20, including:  
said source [contacts] connecting members are double diffused.

24. (Amended) The array configuration of claim 20, including:  
each flash EPROM cell includes a floating gate, the array further including a  
[word line] plurality of word lines each disposed along at least one of the rows, over  
and insulated from the floating gates of the row; and  
and said plurality of [contacts] source connecting members are self-aligned with  
the said word lines and the floating gates of the [row] rows.

*G5*

26. (Amended) The array configuration of claim [25] 20 further comprising [, wherein:  
said means for coupling includes ]  
a plurality of source driver means for coupling at least one source connecting member to  
the erase voltage in response to driver input signal, and  
a source decoder means for generating at least one driver input signal in response to the  
source decode signals.

27. (Amended) The array configuration of claim 26, further including:  
address dependent source decode signal generating means responsive to a  
plurality of memory address signals for generating the source decode signals.

28. (Amended) The array configuration of claim 26, further including:  
user dependent source decode signal generating means responsive to a plurality of  
predefined user values for generating the source decode signals.

29. (Amended) The array configuration of claim 26, further including:  
configurable source decode signal generating means responsive to a plurality of  
predefined user values and memory address values for generating the source decode  
signals.